

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-251866

(43)Date of publication of application : 17.09.1999

---

(51)Int.Cl. H03H 9/25

H03H 3/08

---

(21)Application number : 10-064511 (71)Applicant : TDK CORP

(22)Date of filing : 27.02.1998 (72)Inventor : GOTO MASASHI  
KANAZAWA JITSUO  
KUWAJIMA HAJIME

---

(54) CHIP ELEMENT AND MANUFACTURE OF THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a compact chip element with miniaturized external electrodes and to realize a high-density mounting therein.

SOLUTION: This chip element is obtained by forming an electrode pattern 25 on the main mounting surface 21a of a base material 21 and forming a bump electrode 22 being facedown mounted external electrode. An insulated layer 31 is overlapped with at least a part of the face 21a so as to form an edge part leaving at least a part of the pattern 25 uncovered. A protective layer 32 for protecting the top of the main mounting surface 21a is provided at an interval from the surface 21a, overlapping with the layer 31. The electrode 22 is connected with the pattern 25, while keeping contact with the edge parts of the

layers 32.

---

LEGAL STATUS

[Date of request for examination] 22.10.2002

[Date of sending the examiner's  
decision of rejection] 02.09.2003

[Kind of final disposal of application  
other than the examiner's decision of  
rejection or application converted  
registration]

[Date of final disposal for application]

[Patent number] 3514361

[Date of registration] 23.01.2004

[Number of appeal against examiner's  
decision of rejection] 2003-19247

[Date of requesting appeal against  
examiner's decision of rejection] 02.10.2003

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

**\* NOTICES \***

**JPO and NCIP are not responsible for any  
damages caused by the use of this translation.**

1.This document has been translated by computer. So the translation may not  
reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

3.In the drawings, any words are not translated.

---

## CLAIMS

---

[Claim(s)]

[Claim 1] The chip type element which makes it the description to connect with said electrode pattern while preparing an electrode pattern in the mounting principal plane of a base material, and much more insulating layer which laps with said a part of mounting principal plane [ at least ] is prepared at least so that the edge which it left in the chip type element which prepared the external electrode for face down mounting, without covering said some of electrode patterns [ at least ] may be formed and said external electrode touches said edge of said insulating layer.

[Claim 2] Said insulating layer is a chip type element according to claim 1 which has the 1st insulating layer which forms a frame, and the 2nd insulating layer which laps with this 1st insulating layer, sets a gap to said mounting principal plane, and protects said mounting principal plane top.

[Claim 3] It is the chip type element according to claim 1 or 2 which forms the closed space which said insulating layer avoids said active region, and intervenes between said mounting principal plane and a wearing side substrate by said mounting principal plane having the active region in which the Kushigata electrode for surface acoustic wave devices was formed as said some of electrode patterns, and sticks to the wearing side substrate concerned, and surrounds said active region.

[Claim 4] In the manufacture approach of a chip type element of preparing the external electrode for face down mounting in said mounting principal plane after preparing an electrode pattern in the mounting principal plane of a base material The insulation layer forming process which prepares at least much more insulating layer which laps with said a part of mounting principal plane [ at least ] so that the edge which it left, without covering said some of electrode patterns [ at least ] may be formed by predetermined thickness, The manufacture approach of the chip type element which makes it the description to include the

external electrode formation process which forms the external electrode by which an end is connected to said electrode pattern while touching said edge of said insulating layer.

[Claim 5] The manufacture approach of a chip type element according to claim 4 of making both sides of said mounting principal plane and said wearing side substrate sticking said insulating layer in said face down mounting process after said external electrode formation process while carrying out bonding of said external electrode to a wearing side substrate, having the face down mounting process which carries out face down mounting and connecting said external electrode to the conductor pattern of said wearing side substrate.

---

[Translation done.]

**\* NOTICES \***

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

---

## DETAILED DESCRIPTION

---

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the manufacture approach of chip type elements, such as a surface acoustic wave device by which face down mounting is carried out on wearing side substrates (substrate for mounting), such as a package substrate with which the circuit board and the wiring circuit of

electronic equipment were formed, and a chip type element.

[0002]

[Description of the Prior Art] In recent years, the high-density-assembly method which carries out face down mounting of the bump electrode (external electrode) of various chip type elements, such as not only a semi-conductor but L, C, R, or a surface acoustic wave device, on the circuit board of electronic equipment is spreading. In order to attain small and light-ization of electronic equipment further from now on, the manufacture approach of a chip type element or a chip type element which can carry out [ detailed ]-izing of the bump electrode much more is needed. Hereafter, the conventional technique is explained recently by making into an example the surface acoustic wave device widely used for the mobile wireless device, the navigation system, etc.

[0003] Drawing 6 is the sectional view showing the conventional surface acoustic wave device 1 by which face down mounting was carried out through the bump electrode 2 on the circuit board 10 as a substrate for mounting. The active region 4 equipped with the Kushigata electrode 3 is formed in the mounting principal plane of a surface acoustic wave device 1, and the Kushigata electrode 3 is connected to the conductor pattern 11 of the circuit board 10 through the bump electrode 2 via the electrode pattern which was formed on the mounting principal plane of a surface acoustic wave device and which is not illustrated. In addition, as for the electrode bump 2, the grand pattern of a surface acoustic wave device etc. is connected besides the Kushigata electrode. Thus, face down mounting of the surface acoustic wave device 1 is carried out using the ultrasonic bonding, conductive resin or a pewter, etc. so that an active region 4 may meet the conductor pattern side of the circuit board 10.

[0004] After face down mounting of the surface acoustic wave device 1 as such a chip type element is carried out on the circuit board 10, usually closure protection is carried out with sheathing resin 13, such as an epoxy resin which sets buffer resin 12, such as silicone resin which served both as stress relaxation and an insulation, mechanical protection, and moisture-proof strengthening as the main

purposes.

[0005] However, according to the method which closes the chip type element which carried out face down mounting on the circuit board as mentioned above by resin, the buffer resin which invaded between a chip type element and the circuit board expands by the temperature change, swelling, etc., destroys junction by the detailed bump electrode, and worsens dependability. The resin which invaded between a surface acoustic wave device and the circuit board especially adheres on the surface of an active region, and the engine performance of a surface acoustic wave device is worsened. Then, as shown in drawing 7 or drawing 8, the space which formed and closed the barrage (dam) between the top face of the circuit board and the mounting principal plane of a chip type element was formed, and the device which prevents the influx of resin has been achieved. As the surroundings of an active region 4 are surrounded, drawing 7 is the top view showing the example which forms the dam frame 8, while forming the bump electrode 2 in the mounting principal plane of a surface acoustic wave device 1, and drawing 8 is the top view showing the example which forms the discontinuous barrier 9 in the key point between the bump electrodes 2 prepared in the mounting principal plane of a surface acoustic wave device 1. In addition, the structure of this surface acoustic wave device can see an example to JP,5-55303,A etc.

[0006]

[Problem(s) to be Solved by the Invention] However, in order to miniaturize a chip type element further and to realize high density assembly, such as a reliable multichip onboard, the following unsolved troubles were still left behind also by the above-mentioned conventional technique.

[0007] (1) According to the conventional technique, the barrage and the bump electrode are separately formed on the chip type element. For this reason, the area for forming a barrage was needed on the chip type element, and there was a fault that the configuration of a chip type element will become large as a result since width of face of about 1-several mm is the need for establishing the dam

frame and barrier of sufficient reinforcement.

[0008] (2) Moreover, since the barrage and the bump electrode were formed separately, when the height on both chip type element became irregular and carried out face down mounting of the chip type element on the circuit board, there was a problem that the closed space could not be formed.

[0009] (3) , of course by the discontinuous barrier, the influx of resin cannot be prevented completely.

[0010] (4) In order to advance the miniaturization of a chip type element much more, there is the need of also miniaturizing a bump electrode further again, but if a bump electrode is made a miniaturization, it will become weak in reinforcement.

[0011] Generally, according to the above-mentioned conventional technique, the technical problem that the chip type element which can plan high density assembly by much more miniaturization could not be offered was left behind.

[0012] In addition, while establishing the envelopment wall surrounding the active region of a surface acoustic wave device as another conventional technique, wrap structure is proposed by JP,9-246905,A with the lid in the headroom surrounded with the envelopment wall. However, it is disagreeable \*\*\*\*\* with it difficult [ to enlarge in order to cause enlargement of a component, and for a bump electrode to bear the stress at the time of bonding since a bump electrode is not reinforced with an envelopment wall etc. in the location distant from the envelopment wall, and to obtain necessary fixing reinforcement, since a bump electrode is arranged on the outside of an envelopment wall also in this case, and to advance the miniaturization of a bump electrode ].

[0013] Moreover, since more than one are formed with bonding or a ball on a principal plane according to the above-mentioned conventional technique, it is difficult to arrange the height of two or more bump electrodes.

[0014] When carrying out face down mounting of the chip type element at wearing side substrates, such as the circuit board, this invention If the minimum and a several micrometers gap are left behind between the mounting principal

plane of a chip type element, and the wearing side substrate, will be made based on the knowledge of being enough, and the above-mentioned technical problem is solved. It aims at attaining the miniaturization of the external electrode as a bump electrode etc., and the miniaturization of an appearance, as a result offering the manufacture approach of of the chip type element and chip type element which can realize high density assembly.

[0015] Other purposes and new descriptions of this invention are clarified in the gestalt of the below-mentioned operation.

[0016]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the chip type element of this invention In the configuration which prepared the external electrode for face down mounting while preparing the electrode pattern in the mounting principal plane of a base material While much more insulating layer which laps with said a part of mounting principal plane [ at least ] is prepared at least so that the edge which it left, without covering said some of electrode patterns [ at least ] may be formed, and said external electrode touches said edge of said insulating layer, it is characterized by connecting with said electrode pattern.

[0017] Since the edge of the insulating layer attached with predetermined thickness on the mounting principal plane of a chip type element serves to support an external electrode mechanically according to the chip type element of this invention, it becomes possible to miniaturize the magnitude of an external electrode even in several micrometers thru/or dozens of micrometers for a diameter. In addition, the insulating layer should just constitute not only organic systems, such as an inorganic system (SiO<sub>2</sub>) and polyimide, but \*\*\*\*\*.

Moreover, an external electrode does not carry out a \*\* form independently, and thin film formation, thick-film-paste printing, etc. are sufficient as it.

[0018] In said chip type element, said insulating layer can be considered as the configuration which has the 1st insulating layer which forms a frame, and the 2nd insulating layer which laps with this 1st insulating layer, sets a gap to said

mounting principal plane, and protects said mounting principal plane top.

[0019] Since according to this a mounting principal plane places an opening and is covered with and protected by said 2nd insulating layer, the handling of a chip type element becomes easy, and since adhesion and contamination of a foreign matter can be prevented, the dependability of a chip type element can be raised.

[0020] Moreover, it can also consider as the configuration which forms the closed space which said insulating layer avoids said active region, and intervenes between said mounting principal plane and a wearing side substrate by setting to said chip type element and said mounting principal plane having the active region in which the Kushigata electrode for surface acoustic wave devices was formed as said some of electrode patterns, and sticks to the wearing side substrate concerned, and surrounds said active region.

[0021] Since according to this configuration it works so that it may prevent that in having avoided the active region and having been formed thickness (3 micrometers thru/or about 30 micrometers) of an insulating layer serves as a barrage, for example, and closure resin trespasses upon an active region, after carrying out face down mounting of the surface acoustic wave device on a wearing side substrate, for example with a bare chip, even if it performs a resin seal, the property of a surface acoustic wave device does not worsen.

[0022] [ after the manufacture approach of the chip type element of this invention prepares an electrode pattern in the mounting principal plane of a base material, when preparing the external electrode for face down mounting in said mounting principal plane ] The insulation layer forming process which prepares at least much more insulating layer which laps with said a part of mounting principal plane [ at least ] so that the edge which it left, without covering said some of electrode patterns [ at least ] may be formed by predetermined thickness, The end is characterized by including the external electrode formation process which forms the external electrode connected to said electrode pattern, touching said edge of said insulating layer.

[0023] According to the manufacture approach of the chip type element of this

invention, the edge formed by the insulation layer forming process and the external electrode formed by the external electrode formation process serve to regulate a location and a configuration mutually and to suit.

[0024] In the manufacture approach of the chip type element of this invention, it is good to make both sides of said mounting principal plane and said wearing side substrate stick said insulating layer in said face down mounting process after said external electrode formation process, while carrying out bonding of said external electrode to a wearing side substrate, having the face down mounting process which carries out face down mounting and connecting said external electrode to the conductor pattern of said wearing side substrate.

[0025] In this case, since the edge of an external electrode and an insulating layer is close in case bonding of the external electrode is carried out, it works so that it may reinforce to either deformation, and the bonding strength of an external electrode and a conductor pattern is strengthened. And when adhesive resin is used, it serves for an insulating layer to intervene between a chip type element and a wearing side substrate, to demonstrate a shrinkage force, to attract each other's both, and to raise mounting reinforcement.

[0026]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of the manufacture approach of of the chip type element and chip type element concerning this invention is explained according to a drawing.

[0027] The forward sectional view of a surface acoustic wave device and drawing 3 of a forward sectional view when drawing 1 carries out face down mounting of the surface acoustic wave device as one example of a chip type element at the circuit board as a wearing side substrate (substrate for mounting), and drawing 2 are these top views.

[0028] In these drawings, a surface acoustic wave device 20 has the structure which arranged the electrode pattern 25 which contains the Kushigata electrode 23, the grand pattern which is not illustrated in mounting principal plane 21a which is the single-sided side of the piezo-electric substrates (base material of a

component) 21, such as a lithium-niobate crystal and a lithium tantalate crystal, by aluminum vacuum evaporation etc., and the active region 24 equipped with the Kushigata electrode 23 is formed in mounting principal plane 21a. The electrode pattern part prolonged from said Kushigata electrode 23, grand pattern, etc. forms the pad 33 like drawing 3 .

[0029] On the mounting principal plane of a surface acoustic wave device 20, an active region 24 is avoided and the insulating layer 31 (the 1st insulating layer) and the protective layer 32 (the 2nd insulating layer) are formed as an insulating layer which carries out a laminating and uses insulating resin as a principal component. That is, the surroundings of an active region 24 are surrounded and the insulating layer 31 which thickness becomes from the polyimide resin which is about 5 micrometers is formed in the shape of a frame on the mounting principal plane. An insulating layer 31 is formed by having extended from some pads 33 to even besides a pad, for example, carrying out pattern NINGU of the photosensitive polyimide resin. The space which the protective layer 32 which wrap thickness becomes from the polyimide resin which is about 20 micrometers is formed, and closed the active-region 24 top on the active region 24 is formed by making the insulating layer 31 of the shape of this frame into a spacer. This protective layer 32 is formed by sticking a photosensitive dry film in piles on an insulating layer 31. The protective layer 32 separated space on the active region 24, the active region 24 is covered, and a desirable pure non-oxidizing quality thru/or inert gas is enclosed in a wrap closed space in the active region 24.

[0030] The bump electrode 22 as an external electrode is what functions as an electrode for junction. It is what is arranged at the edge (that is, frame-like part surrounding an active region 24) of an insulating layer which consists of an insulating layer 31 and a protective layer 32. It is [ the bore established by penetrating the edge of an insulating layer 31 and a protective layer 32 ] close, and it is prepared in the insulating layer 31 and protective layer 32 which are formed as a wall of a hole 34 inside the hole 34 which is about 10 micrometers. As for this bump electrode 22, metals, such as copper, and nickel, gold, are

formed of sputtering, vacuum evaporation or electrolysis through hole plating, etc. And it connects with the pad 33 formed in mounting principal plane 20a of a surface acoustic wave device 20 electrically, and the end of the bump electrode 22 is connected to the Kuchigata electrode 23, the grand pattern which is not illustrated via the pad 33.

[0031] Next, drawing 4 (A) - (D) explains the process which carries out face down mounting of the surface acoustic wave device 20 as a chip type element of drawing 1 and drawing 3 on the circuit board.

[0032] Like drawing 4 (A), a surface acoustic wave device 20 has the bump electrode 22 which penetrated the edge of the insulating resin layer which consists of an insulating layer 31 and a protective layer 32, as shown in this drawing (B), on the circuit board 10, the conductor pattern 11 for mounting a surface acoustic wave device 20 is formed, and the bump electrode 22 of a surface acoustic wave device 20 is positioned according to the location of a conductor pattern 11. Then, a supersonic wave and thrust are applied to the bump electrode 22 by the ultrasonic bonder, for example, and as shown in this drawing (C), a part of bump electrode 22, insulating layer 31, and protective layer 32 deform, and the bump electrode 22 and the conductor pattern 11 of the circuit board 10 are close, and are joined. At this time, an insulating layer 31 or a protective layer 32 sticks a surface acoustic wave device 20 to the circuit board 10, and face down bonding is carried out. In addition, since an active region 24 separates the sealed space and is protected by the protective layer 32, it is not influenced by bonding.

[0033] Moreover, as shown in this drawing (D), by making adhesives (new adhesive resin layer) 35 intervene between a protective layer 32 and the circuit board 10, adhesive strength and a shrinkage force peculiar to a macromolecule are used, and a surface acoustic wave device 20 can also be reinforced on the circuit board, and it can also fix. When using adhesives 35 together, it is good also as a configuration which omits a protective layer.

[0034] Like drawing 1, after connecting the bump electrode 22 to the conductor

pattern 11 of the circuit board 10 by bonding through opening of a protective layer 32 from an insulating layer 31, closure protection of the surface acoustic wave device 20 top which carried out face down mounting if needed is carried out with the buffer resin 12 and the sheathing resin 13 which were prolonged even on the circuit board. Buffer resin 12 is silicone resin which served both as stress relaxation and an insulation, and sheathing resin 13 is an epoxy resin which sets mechanical protection and moisture-proof strengthening as the main purposes.

[0035] Next, the manufacture approach of the surface acoustic wave device 20 as a chip type element shown in drawing 1 thru/or drawing 4 with reference to drawing 5 is explained. After thickness forms the electrode pattern (pattern for various electrodes and wiring) 25 which are 500 thru/or 2000Å by aluminum vacuum evaporation etc. on the component substrate 21 which is a lithium tantalate single crystal substrate whose thickness of drawing 5 (A) is 0.35mm thru/or 0.5mm, The insulating layer 31 which carried out pattern NINGU of the photosensitive polyimide resin whose thickness is 5 micrometers as shown in this drawing (B), and left it is formed, and the space which carried out the laminating of the protective layer 32 which consists an insulating layer 31 of polyimide resin whose thickness is 25 micrometers as a spacer as shown in this drawing (C), and was closed on the active region is formed. Then, as shown in this drawing (D), the diameter of up opening establishes the hole 34 which is 20 micrometers to the polyimide resin of a protective layer 32. And the metal layers 35 (chromium serves as the lowest layer and gold usually serves as the maximum upper layer), such as chromium, copper, nickel, and gold, are deposited by electrolytic plating, vacuum evaporation, etc. so that a top face may be covered, as shown in this drawing (E). In addition, since the closure of the top face of the active region 24 by the side of a mounting principal plane is carried out by the protective layer 32, it also has the special advantage that it can plate. Then, as shown in this drawing (F), pattern removal of the metal layer 35 is carried out by etching etc., and the bump electrode 22 whose up outer diameter is about 40 micrometers is formed.

[0036] According to the gestalt of this operation, the effectiveness as follows can be acquired.

[0037] (1) Since the bump electrode 22 as an external electrode is formed in the edge of an insulating layer (the gestalt of this operation insulating resin layer) which consists of an insulating layer 31 and a protective layer 32, it can attain the miniaturization of the configuration of a chip type element as compared with the structure which arranges a bump electrode on the outside of the conventional dam frame or a barrier.

[0038] (2) Since the bump electrode 22 is formed where the edge of an insulating layer is touched, and it is reinforced with an insulating layer, it is possible to make the path of the bump electrode 22 thin. Moreover, the bonding strength between the bump electrode 22 and the circuit board side conductor pattern 11 can be strengthened by considering as the structure which an insulating layer sticks and pastes up on a circuit board side in the case of the face down bonding to the circuit board 10 by the bump electrode 22.

[0039] (3) While surrounding an active region 24 by the frame-like insulating layer 31, the seal space by which separated the 5-micrometer gap and the closure was carried out to the open air by closing the headroom of an active region 24 by the protective layer 32 on the active region 24 is formed. When the closure of the surface acoustic wave device was carried out and it was conventionally intercepted from the external world neither with glassware nor a ceramic package, few humidity and foreign matters adhered on the surface of the active region, the property had deteriorated, but according to the configuration of the gestalt of this operation, since the closure of the active region 24 is covered with and carried out by the protective layer 32, property degradation etc. is not caused on handling. Even if this is not restricted to the gestalt of this operation which made the surface acoustic wave device the example but applies this invention to a semiconductor chip, it is the same.

[0040] (4) By forming two or more bump electrodes 22 in coincidence with membrane formation techniques, such as a thin film technology and plating, the

height of two or more bump electrodes 22 can be arranged.

[0041] Although the approach using a photosensitive dry film was mentioned as the example as an approach of forming a protective layer with the gestalt of the above-mentioned implementation, hole processing is carried out beforehand at the bonding sheet using the polyimide film which has an adhesive property besides this approach, and a sheet [ finishing / this processing ] may be stuck on an insulating layer.

[0042] Moreover, laser may be used and a hole may be processed, after sticking the bonding sheet using a polyimide film with the adhesive property which has not carried out hole processing etc.

[0043] Moreover, an anisotropy electric conduction sheet may be used as a protective layer. In this case, after carrying out pattern NINGU of the insulating layer, forming it and forming a bump electrode further, a protective layer is formed by covering an insulating layer and a bump electrode and sticking an anisotropy electric conduction sheet. Since an anisotropy electric conduction sheet can be pasted up on the whole surface when such a chip type element is mounted in the circuit board, seal nature without airtight leakage is obtained.

[0044] Furthermore, in the gestalt of the above-mentioned implementation, although the bump electrode illustrated the case where a tip head was a flat side, the configuration where the center section was dented etc. is sufficient as it. Moreover, although the head illustrated the broad configuration as compared with the base as a bump electrode, the configuration of the size same from a base to a tip head etc. is sufficient.

[0045] Since the structure shown with the gestalt of the above-mentioned implementation, then the mounting principal plane of a chip type element will be covered with a protective layer, bump ingredients with which varieties differ, such as solder metallurgy and conductive resin, can be used for the bump electrode of a chip type element, and, moreover, various connection types, such as cream solder and an ultrasonic bonding by conductive resin and gold, can be used for it. Consequently, in case various kinds of chip type elements are mounted on the

same circuit board, various chip type elements -- a certain chip type element mounts with solder, and other chip type elements perform mounting by electroconductive glue -- can be mounted by the various junction approaches on the same circuit board at coincidence. And the ambient atmosphere at the time of junction, temperature, reflow conditions, ultrasonic-bonding conditions, etc. can be selected broadly. That is, according to this invention, the outstanding effectiveness that it becomes easy to carry out MCM mounting of the chip type element from which plurality differs on the same circuit board freely is induced. [0046] In addition, since the whole can also be covered by sheathing resin after carrying out MCM mounting of the chip type element of the gestalt of this operation on the circuit board, various deformation, such as making [ an abbreviation thru/or ] a protective layer simple and carrying out the resin seal of the outside finally, is possible.

[0047] Although the gestalt of operation of this invention has been explained above, probably, as for this invention, it will be obvious to this contractor for various kinds of deformation and modification to be possible within the limits of the publication of a claim, without being limited to this.

[0048]

[Effect of the Invention] Since according to this invention it is close to the edge of an insulating layer established in the mounting principal plane of the chip type element by which face down mounting is carried out and the external electrode was prepared on the wearing side substrate as explained above, a chip type element can be miniaturized and the chip type element in which the high density assembly moreover equipped with high dependability is possible can be offered. Moreover, the small surface acoustic wave device excellent in dependability can be offered by applying this invention to a surface acoustic wave device.

[0049] Furthermore, since the insulation layer forming process and the external electrode formation process which produces an external electrode in contact with an insulating layer were formed according to the manufacture approach of this

invention, it is effective in the ability to form the chip type element which has a minute external electrode.

---

[Translation done.]

\* NOTICES \*

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.\*\*\*\* shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

---

## DESCRIPTION OF DRAWINGS

---

[Brief Description of the Drawings]

[Drawing 1] It is the gestalt of operation of this invention and is the sectional view showing the condition of having carried out face down mounting of the chip type element at the circuit board.

[Drawing 2] It is the forward sectional view of the chip type element in the gestalt of operation.

[Drawing 3] It is this top view.

[Drawing 4] It is the expanded sectional view showing the structure of the bump electrode circumference prepared in the chip type element, and the procedure of face down bonding.

[Drawing 5] It is the explanatory view showing the manufacture procedure of a chip type element.

[Drawing 6] It is the sectional view showing the conventional example of a chip type element.

[Drawing 7] It is the top view showing the conventional example similarly.

[Drawing 8] It is the top view showing other conventional examples of a chip type element.

[Description of Notations]

1 20 Surface acoustic wave device

2 22 Bump electrode

3 23 Kushigata electrode

4 24 Active region

10 Circuit Board

11 Conductor Pattern

12 Buffer Resin

13 Sheathing Resin

21 Piezo-electric Substrate

21a Mounting principal plane

25 Electrode Pattern

31 Insulating Layer

32 Protective Layer

33 Pad

34 Hole

---

[Translation done.]

**\* NOTICES \***

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

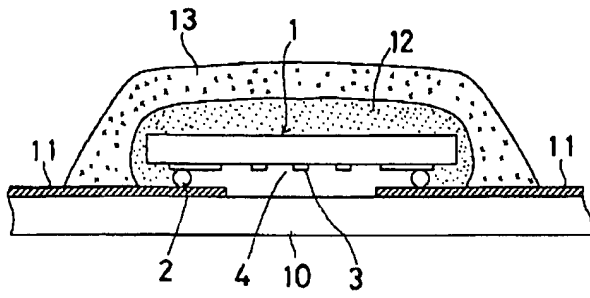
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.\*\*\*\* shows the word which can not be translated.

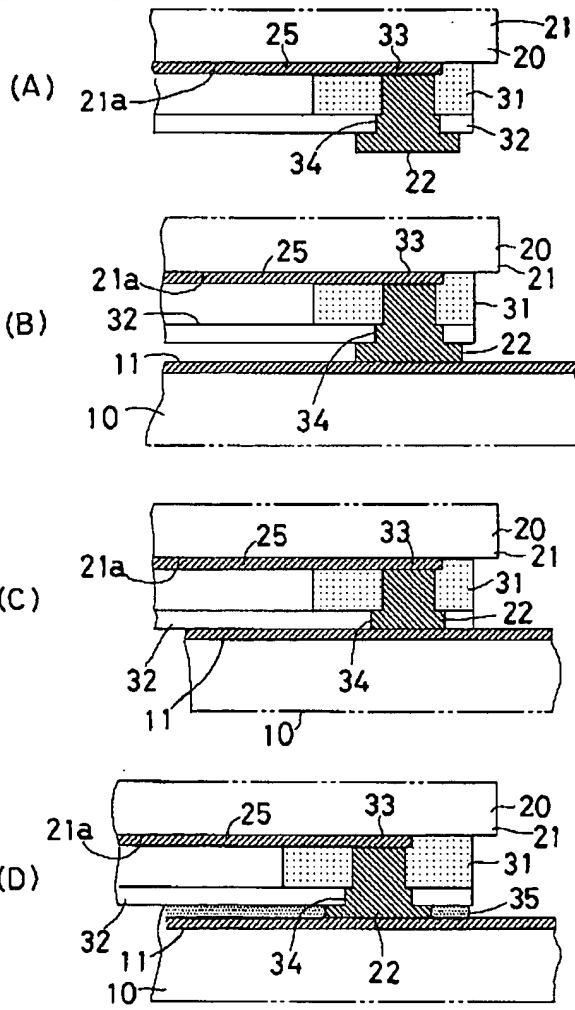
3.In the drawings, any words are not translated.



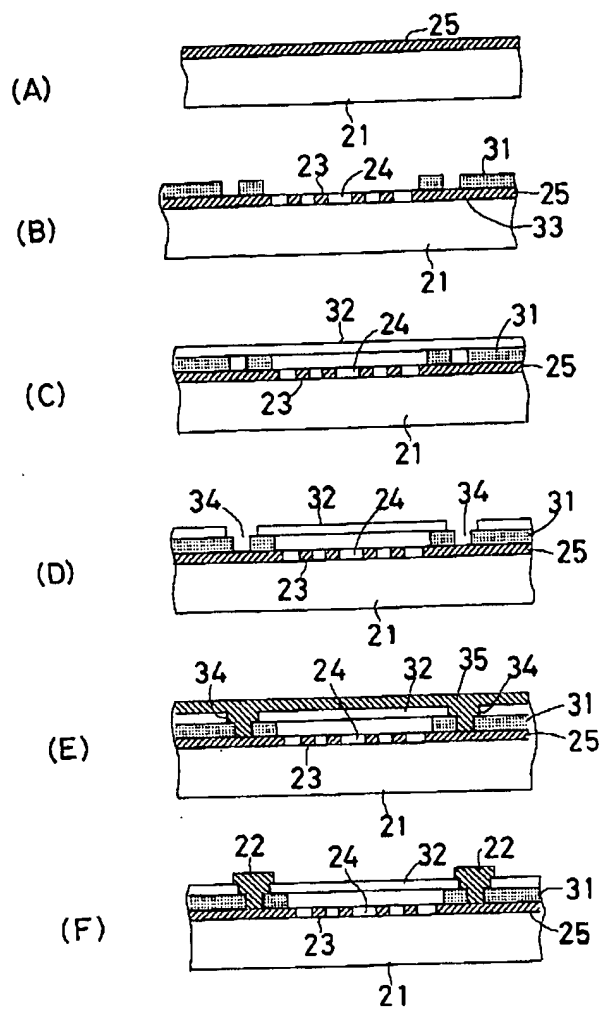




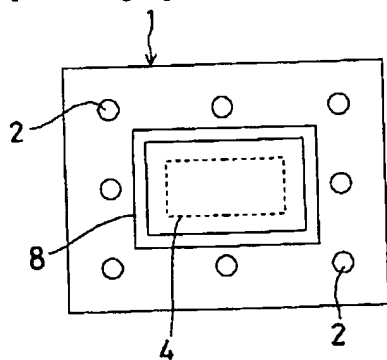
[Drawing 4]



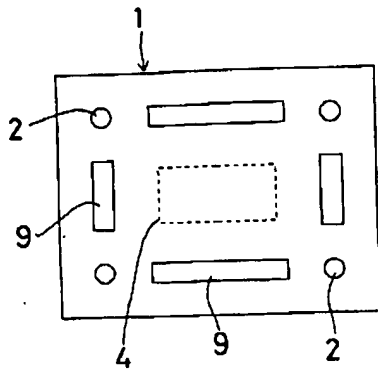
[Drawing 5]



[Drawing 7]



[Drawing 8]



---

[Translation done.]

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-251866

(43)Date of publication of application : 17.09.1999

(51)Int.Cl.

H03H 9/25  
H03H 3/08

(21)Application number : 10-064511

(71)Applicant : TDK CORP

(22)Date of filing : 27.02.1998

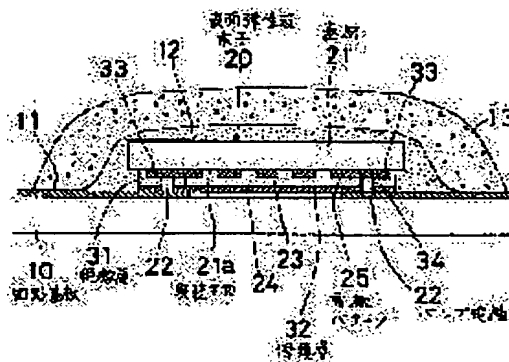
(72)Inventor : GOTO MASASHI  
KANAZAWA JITSUO  
KUWAJIMA HAJIME

## (54) CHIP ELEMENT AND MANUFACTURE OF THE SAME

## (57)Abstract:

**PROBLEM TO BE SOLVED:** To obtain a compact chip element with miniaturized external electrodes and to realize a high-density mounting therein.

**SOLUTION:** This chip element is obtained by forming an electrode pattern 25 on the main mounting surface 21a of a base material 21 and forming a bump electrode 22 being facedown mounted external electrode. An insulated layer 31 is overlapped with at least a part of the face 21a so as to form an edge part leaving at least a part of the pattern 25 uncovered. A protective layer 32 for protecting the top of the main mounting surface 21a is provided at an interval from the surface 21a, overlapping with the layer 31. The electrode 22 is connected with the pattern 25, while keeping contact with the edge parts of the layers 32.



## LEGAL STATUS

[Date of request for examination]	22.10.2002
[Date of sending the examiner's decision of rejection]	02.09.2003
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3514361
[Date of registration]	23.01.2004
[Number of appeal against examiner's decision of rejection]	2003-19247
[Date of requesting appeal against examiner's decision of rejection]	02.10.2003
[Date of extinction of right]	

Copyright (C); 1998,2003 Japan Patent Office

(19) 日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開平 1 1 - 2 5 1 8 6 6

(43) 公開日 平成 11 年 (1999) 9 月 17 日

(51) Int. Cl.<sup>6</sup>

識別記号

F I

H 0 3 H 9/25

H 0 3 H 9/25

A

3/08

3/08

審査請求 未請求 請求項の数 5

F D

(全 7 頁)

(21) 出願番号 特願平 10-64511

(22) 出願日 平成 10 年 (1998) 2 月 27 日

(71) 出願人 000003067

ティーディーケイ株式会社

東京都中央区日本橋一丁目 13 番 1 号

(72) 発明者 後藤 真史

東京都中央区日本橋一丁目 13 番 1 号ティー  
ディーケイ株式会社内

(72) 発明者 金澤 實雄

東京都中央区日本橋一丁目 13 番 1 号ティー  
ディーケイ株式会社内

(72) 発明者 桑島

東京都中央区日本橋一丁目 13 番 1 号ティー  
ディーケイ株式会社内

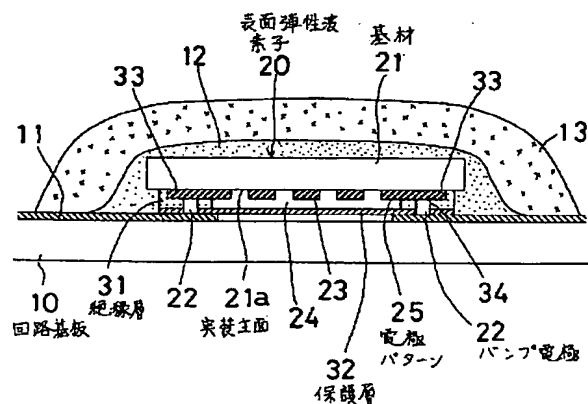
(74) 代理人 弁理士 村井 隆

(54) 【発明の名称】 チップ素子及びチップ素子の製造方法

(57) 【要約】

【課題】 外部電極の小型化、外形の小型化を図り、ひいては高密度実装を実現可能なチップ素子を提供する。

【解決手段】 基材 21 の実装主面 21a に電極パターン 25 を設けるとともにフェースダウン実装用外部電極としてのパンプ電極 22 を設けたチップ素子において、電極パターン 25 の少なくとも一部を覆わずに残した縁部が形成されるように実装主面 21a の少なくとも一部に重なる絶縁層 31 を設け、さらに絶縁層 31 に重なって実装主面 21a に対して間隙をおいて実装主面上を保護する保護層 32 を設け、前記パンプ電極 22 が前記絶縁層 31 及び保護層 32 の縁部に接しながら電極パターン 25 に接続された構成となっている。



## 【特許請求の範囲】

【請求項 1】 基材の実装主面に電極パターンを設けるとともにフェースダウン実装用の外部電極を設けたチップ素子において、

前記電極パターンの少なくとも一部を覆わずに残した縁部が形成されるように前記実装主面の少なくとも一部に重なる少なくとも一層の絶縁層を設け、前記外部電極が前記絶縁層の前記縁部に接しながら前記電極パターンに接続されていることを特徴とするチップ素子。

【請求項 2】 前記絶縁層は、枠体を形成する第 1 の絶縁層と、該第 1 の絶縁層に重なって前記実装主面に対して間隙をおいて前記実装主面上を保護する第 2 の絶縁層とを有する請求項 1 記載のチップ素子。

【請求項 3】 前記実装主面は、前記電極パターンの一部として表面弾性波素子用の櫛形電極が形成された活性領域を有しており、前記絶縁層は前記活性領域を避けて前記実装主面と装着側基板間に介在しかつ当該装着側基板に密着して前記活性領域を囲む閉空間を形成する請求項 1 又は 2 記載のチップ素子。

【請求項 4】 基材の実装主面に電極パターンを設けた後、フェースダウン実装用の外部電極を前記実装主面に設けるチップ素子の製造方法において、

前記電極パターンの少なくとも一部を覆わずに残した縁部が形成されるように前記実装主面の少なくとも一部に重なる少なくとも一層の絶縁層を所定厚さで設ける絶縁層形成工程と、

前記絶縁層の前記縁部に接しながら一端が前記電極パターンに接続される外部電極を形成する外部電極形成工程とを含むことを特徴とするチップ素子の製造方法。

【請求項 5】 前記外部電極形成工程後に、前記外部電極を装着側基板にボンディングしてフェースダウン実装するフェースダウン実装工程を有し、前記外部電極を前記装着側基板の導体パターンに接続させるとともに、前記フェースダウン実装工程において前記実装主面と前記装着側基板との両面に前記絶縁層を密着させる請求項 4 記載のチップ素子の製造方法。

## 【発明の詳細な説明】

## 【0001】

【発明の属する技術分野】本発明は、電子機器の回路基板や配線回路が形成されたパッケージ基板等の装着側基板（実装対象基板）上にフェースダウン実装される表面弾性波素子等のチップ素子及びチップ素子の製造方法に関する。

## 【0002】

【従来の技術】近年、半導体だけでなく、L、C、Rあるいは表面弾性波素子等の各種チップ素子のバンプ電極（外部電極）を電子機器の回路基板上にフェースダウン実装する高密度実装方式が普及しつつある。今後さらに電子機器の軽薄短小化を図るためには、バンプ電極を一段と微細化できるチップ素子やチップ素子の製造方法が

必要になる。以下、最近、移動体無線機器やナビゲーションシステム等に広く用いられている表面弾性波素子を例として従来技術を説明する。

【0003】図 6 は、実装対象基板としての回路基板 10 上にバンプ電極 2 を介してフェースダウン実装された従来の表面弾性波素子 1 を示す断面図である。表面弾性波素子 1 の実装主面には櫛形電極 3 を備えた活性領域 4 が形成されており、櫛形電極 3 は表面弾性波素子の実装主面上に形成された図示されぬ電極パターンを経由し、バンプ電極 2 を介して回路基板 10 の導体パターン 11 に接続されている。なお、電極バンプ 2 は、櫛形電極以外にも表面弾性波素子のグランドパターン等も接続されている。このようにして、表面弾性波素子 1 は活性領域 4 が回路基板 10 の導体パターン面に対面するように超音波ボンディングや導電性樹脂、あるいはハンダ等を用いてフェースダウン実装されている。

【0004】このようなチップ素子としての表面弾性波素子 1 は、回路基板 10 上にフェースダウン実装されたのち、応力緩和と絶縁を兼ねたシリコン樹脂等のバッファ樹脂 12 や、機械的な保護や耐湿強化を主な目的とするエポキシ樹脂等の外装樹脂 13 によって封止保護されるのが通常である。

【0005】しかしながら、上記のように回路基板上にフェースダウン実装したチップ素子を樹脂で封止する方式によれば、チップ素子と回路基板の間に侵入したバッファ樹脂が温度変化や膨潤等により膨張し、微細なバンプ電極による接合を破壊して信頼性を悪くする。特に、表面弾性波素子と回路基板の間に侵入した樹脂が活性領域の表面に付着し、表面弾性波素子の性能を悪化させる。そこで、図 7 や図 8 に示すように、回路基板の上面とチップ素子の実装主面との間に堰堤（ダム）を設けて閉じた空間を形成し、樹脂の流れ込みを防ぐ工夫が図られてきた。図 7 は表面弾性波素子 1 の実装主面にバンプ電極 2 を設けるとともに活性領域 4 の周りを取り囲むようにダム枠 8 を設ける例を示す平面図であり、図 8 は表面弾性波素子 1 の実装主面に設けたバンプ電極 2 の間の所要所に不連続な防壁 9 を形成する例を示す平面図である。なお、かかる表面弾性波素子の構造は、特開平 5-55303 号公報等にも例を見ることができる。

## 【0006】

【発明が解決しようとする課題】しかしながら、チップ素子をさらに小型化して信頼性の高いマルチチップオンボード等の高密度実装を実現するためには、上記の従来技術によっても、依然、次のような未解決な問題点が残されていた。

【0007】(1) 従来技術によれば、堰堤とバンプ電極はチップ素子上に別々に形成されている。このため、堰堤を設けるための面積がチップ素子上に必要になり、十分な強度のダム枠や防壁を設けるには 1 ～数 mm 程度の幅が必要なので、結果としてチップ素子の形状が大きく

なってしまうという欠点があった。

【0008】(2) また、堰堤とパンプ電極は別々に形成されるので、両者のチップ素子上での高さが不揃いになり、回路基板上にチップ素子をフェースダウン実装した場合に、閉じた空間を形成できないという問題があった。

【0009】(3) もちろん、不連続な防壁では樹脂の流れ込みを完全には防ぐことができない。

【0010】(4) さらにまた、チップ素子の小型化を一段と進めるには、パンプ電極も小型化する必要が有るが、パンプ電極を小型化にすると強度的に弱くなる。

【0011】総じて、上記の従来技術によれば、一層の小型化により高密度実装を図ることが可能なチップ素子を提供することができないという課題が残されていた。

【0012】なお、別の従来技術として、表面弾性波素子の活性領域を囲む包囲壁を設けるとともに包囲壁で囲まれた上方空間を蓋体で覆う構造が特開平 9-246905号で提案されている。しかし、この場合にも包囲壁の外側にパンプ電極を配置するので素子の大型化を招き、またパンプ電極は包囲壁から離れた位置で包囲壁等によって補強されないため、パンプ電極はボンディング時の応力に耐え、かつ所要の固着強度を得るために大きくする必要があり、パンプ電極の小型化を進めることが困難なきらいがある。

【0013】また、上記従来技術によると、主面上に複数個ボンディング又はボール等によって形成しているので、複数のパンプ電極の高さを揃えることが困難である。

【0014】この発明は、回路基板等の装着側基板にチップ素子をフェースダウン実装する場合に、チップ素子の実装主面と装着側基板との間に最小限、数 $\mu\text{m}$ の間隙が残されておれば十分であるという知見に基づいてなされたものであり、上記の課題を解決して、パンプ電極等としての外部電極の小型化、外形の小型化を図り、ひいては高密度実装を実現可能なチップ素子及びチップ素子の製造方法を提供することを目的とする。

【0015】本発明のその他の目的や新規な特徴は後述の実施の形態において明らかにする。

【0016】

【課題を解決するための手段】上記目的を達成するために、本発明のチップ素子は、基材の実装主面に電極パターンを設けるとともにフェースダウン実装用の外部電極を設けた構成において、前記電極パターンの少なくとも一部を覆わずに残した縁部が形成されるように前記実装主面の少なくとも一部に重なる少なくとも一層の絶縁層を設け、前記外部電極が前記絶縁層の前記縁部に接しながら前記電極パターンに接続されていることを特徴としている。

【0017】本発明のチップ素子によれば、チップ素子の実装主面上に所定の厚さをもって重着された絶縁層の

縁部が外部電極を機械的に支える働きをするので、外部電極の大きさを例えば直径で数 $\mu\text{m}$ 乃至数十 $\mu\text{m}$ にまで小型化することが可能になる。なお、絶縁層は無機系(SiO<sub>2</sub>)やポリイミド等の有機系に限らず、絶縁層をを構成していればよい。また、外部電極は独立して保形できる必要はなく、薄膜形成や厚膜ペースト印刷等でもよい。

【0018】前記チップ素子において、前記絶縁層は、枠体を形成する第1の絶縁層と、該第1の絶縁層に重なって前記実装主面に対して間隙をおいて前記実装主面上を保護する第2の絶縁層とを有する構成とすることができ。

【0019】これによれば、実装主面は空隙を置いて前記第2の絶縁層によって覆われて保護されるので、チップ素子の取り扱いが容易になり、異物の付着や汚染を防ぐことができるのでチップ素子の信頼性を高めることができる。

【0020】また、前記チップ素子において、前記実装主面は、前記電極パターンの一部として表面弾性波素子用の櫛形電極が形成された活性領域を有しており、前記絶縁層は前記活性領域を避けて前記実装主面と装着側基板間に介在しかつ当該装着側基板に密着して前記活性領域を囲む閉空間を形成する構成とすることもできる。

【0021】この構成によれば、活性領域を避けて形成された例えば3 $\mu\text{m}$ 乃至30 $\mu\text{m}$ 程度の厚さの絶縁層が堰堤となって封止樹脂が活性領域へ侵入するのを阻止するように働くので、例えば表面弾性波素子をベアチップのまま装着側基板上にフェースダウン実装したのちに樹脂封止を行っても表面弾性波素子の特性が悪くなるということが無い。

【0022】本発明のチップ素子の製造方法は、基材の実装主面に電極パターンを設けた後、フェースダウン実装用の外部電極を前記実装主面に設ける場合において、前記電極パターンの少なくとも一部を覆わずに残した縁部が形成されるように前記実装主面の少なくとも一部に重なる少なくとも一層の絶縁層を所定厚さで設ける絶縁層形成工程と、前記絶縁層の前記縁部に接しながら一端が前記電極パターンに接続される外部電極を形成する外部電極形成工程とを含むことを特徴としている。

【0023】本発明のチップ素子の製造方法によれば、絶縁層形成工程により形成された縁部と、外部電極形成工程によって形成される外部電極とは、互いに位置や形状を規制しあう働きをする。

【0024】本発明のチップ素子の製造方法において、前記外部電極形成工程後に、前記外部電極を装着側基板にボンディングしてフェースダウン実装するフェースダウン実装工程を有し、前記外部電極を前記装着側基板の導体パターンに接続させるとともに、前記フェースダウン実装工程において前記実装主面と前記装着側基板との両面に前記絶縁層を密着させるとよい。

【0025】この場合、外部電極をボンディングする際に外部電極と絶縁層の縁部が密接しているため、何れか一方の変形に対して補強するように働き、外部電極と導体パターンの接合強度を強める。しかも、接着性の樹脂を用いた場合、絶縁層がチップ素子と装着側基板の間に介在して収縮力を発揮し、両者を引き付け合せて実装強度を高める働きをする。

【0026】

【発明の実施の形態】以下、本発明に係るチップ素子及びチップ素子の製造方法の実施の形態を図面に従って説明する。

【0027】図1はチップ素子の一具体例としての表面弾性波素子を装着側基板（実装対象基板）としての回路基板にフェースダウン実装した場合の正断面図、図2は表面弾性波素子の正断面図、図3は同平面図である。

【0028】これらの図において、表面弾性波素子20は、ニオブ酸リチウム結晶やタンタル酸リチウム結晶等の圧電基板（素子の基材）21の片側面である実装主面21aに、アルミ蒸着等により櫛形電極23、図示しないグラウンドパターン等を含む電極パターン25を配した構造を有し、実装主面21aには櫛形電極23を備えた活性領域24が形成されている。前記櫛形電極23やグラウンドパターン等から延びた電極パターン部分は図3の如くパッド33を形成している。

【0029】表面弾性波素子20の実装主面上には、活性領域24を避けて絶縁層31（第1の絶縁層）と保護層32（第2の絶縁層）が積層して絶縁性樹脂を主成分とする絶縁層として設けられている。すなわち、活性領域24の周りを囲んで、厚さが5 $\mu$ m程度のポリイミド樹脂からなる絶縁層31が実装主面上に枠状に設けられている。絶縁層31はパッド33の一部からパッド外にまで延びており、例えば感光性のポリイミド樹脂をパターンニングすることにより形成される。この枠体状の絶縁層31をスペーサーとして活性領域24の上を覆う厚さが20 $\mu$ m程度のポリイミド樹脂からなる保護層32が設けられており、活性領域24上に閉じた空間を形成している。この保護層32は例えば絶縁層31の上に感光性ドライフィルムを重ねて貼ることによって形成される。保護層32は活性領域24の上では空間を隔てて活性領域24を覆っており、活性領域24を覆う密閉空間内は好ましくは清浄な非酸化性乃至不活性気体が封入されている。

【0030】外部電極としてのバンプ電極22は、接合用電極として機能するもので、絶縁層31と保護層32からなる絶縁層の縁部（つまり活性領域24を囲む枠体状部分）に配置されるもので、絶縁層31と保護層32の縁部を貫通して開設された内径が10 $\mu$ m程度の穴34の内側に、穴34の内壁として形成される絶縁層31と保護層32に密接して設けられている。このバンプ電極22は銅やニッケル、金等の金属がスパッタリングや

蒸着又は電解スルーホールメッキ等により形成されている。そして、バンプ電極22の一端は、表面弾性波素子20の実装主面20aに形成されるパッド33に電気的に接続し、パッド33を経由して櫛形電極23や図示されぬグラウンドパターン等に接続されている。

【0031】次に、図1及び図3のチップ素子としての表面弾性波素子20を回路基板上にフェースダウン実装する過程を図4（A）～（D）で説明する。

【0032】図4（A）の如く表面弾性波素子20は絶縁層31と保護層32とからなる絶縁樹脂層の縁部を貫通したバンプ電極22を有し、同図（B）の如く回路基板10上には、表面弾性波素子20を実装するための導体パターン11が設けられており、表面弾性波素子20のバンプ電極22が導体パターン11の位置に合わせて位置決めされる。その後、例えば超音波ボンダーによりバンプ電極22に超音波と押圧力が加えられ、同図

（C）のようにバンプ電極22や絶縁層31、保護層32の一部が変形してバンプ電極22と回路基板10の導体パターン11が密接して接合される。このとき、表面弾性波素子20は絶縁層31あるいは保護層32が回路基板10に密着してフェースダウンボンディングされる。なお、活性領域24は密閉された空間を隔てて保護層32により保護されているのでボンディングによって影響を受けることがない。

【0033】また、同図（D）のように、保護層32と回路基板10との間に接着剤（新たな接着性樹脂層）35を介在させることにより、接着力と高分子に特有な収縮力を利用して、表面弾性波素子20を回路基板上に補強、固定することもできる。接着剤35を併用する場合、保護層を省略する構成としてもよい。

【0034】図1のように、バンプ電極22を絶縁層31から保護層32の開口部を経て回路基板10の導体パターン11にボンディングで接続した後、必要に応じてフェースダウン実装した表面弾性波素子20の上を回路基板上にまで延びたバフファ樹脂12と外装樹脂13によって封止保護する。バフファ樹脂12は応力緩和と絶縁を兼ねたシリコン樹脂等であり、外装樹脂13は機械的な保護や耐湿強化を主な目的とするエポキシ樹脂等である。

【0035】次に図5を参照して図1乃至図4に示したチップ素子としての表面弾性波素子20の製造方法を説明する。図5（A）の厚さが0.35mm乃至0.5mmのタンタル酸リチウム単結晶基板である素子基板21上にアルミ蒸着等により厚が500乃至2000オングストロームの電極パターン（各種電極及び配線のためのパターン）25を形成した後、同図（B）のように厚さが5 $\mu$ mの感光性ポリイミド樹脂をパターンニングして残した絶縁層31を形成し、同図（C）のように絶縁層31をスペーサーとして厚さが25 $\mu$ mのポリイミド樹脂からなる保護層32を積層して活性領域上に閉じた空間を

形成する。その後、同図 (D) の如く保護層 32 のポリイミド樹脂に上部開口径が  $20\mu\text{m}$  の穴 34 を開設する。そして、同図 (E) のように上面を覆うように電解メッキや蒸着等によりクロム、銅、ニッケル、金等の金属層 35 (通常クロムが最下層、金が最上層となる) を堆積する。なお、実装主面側の活性領域 24 の上面は保護層 32 によって封止されているので、メッキを行うことができるという特別な利点もある。その後、同図

(F) の如く金属層 35 をエッチング等によりパターン除去して上部外径が  $40\mu\text{m}$  程度のパンプ電極 22 を形成する。

【0036】この実施の形態によれば、次の通りの効果を得ることができる。

【0037】(1) 外部電極としてのパンプ電極 22 は絶縁層 31 と保護層 32 とからなる絶縁層 (本実施の形態では絶縁樹脂層) の縁部に設けるため、従来のダム枠や防壁の外側にパンプ電極を配置する構造に比してチップ素子の形状の小型化を図ることができる。

【0038】(2) パンプ電極 22 は絶縁層の縁部に接した状態で形成され、絶縁層で補強されるから、パンプ電極 22 の径を細くすることが可能である。また、パンプ電極 22 による回路基板 10 へのフェースダウンボンディングの際に回路基板側に絶縁層が密着して接着する構造とすることで、パンプ電極 22 と回路基板側導体パターン 11 間の接合強度を強めることができる。

【0039】(3) 枠体状の絶縁層 31 で活性領域 24 を囲むとともに、活性領域 24 の上方空間を保護層 32 で閉じることで、活性領域 24 上に  $5\mu\text{m}$  の間隙を隔てて外気に対して封止された密封空間が形成されている。従来は表面弾性波素子がガラス容器やセラミックパッケージ等によって封止されて外界から遮断されない場合には、僅かな湿度や異物が活性領域の表面に付着して特性が劣化していたが、本実施の形態の構成によれば、活性領域 24 は保護層 32 によって覆われて封止されるので、取り扱い上でも特性劣化等をきたさない。このことは、表面弾性波素子を例とした本実施の形態に限られず、半導体チップに本発明を適用しても同様である。

【0040】(4) 複数のパンプ電極 22 を薄膜技術やメッキ等の成膜技術で同時に形成することで、複数のパンプ電極 22 の高さを揃えることができる。

【0041】上記実施の形態では、保護層を形成する方法として、感光性のドライフィルムを用いる方法を例に挙げたが、この方法以外にも、例えば、接着性のあるポリイミドフィルム等を用いたボンディングシートに予め穴加工し、この加工済みのシートを絶縁層に貼り合わせても良い。

【0042】また、穴加工していない接着性のあるポリイミドフィルム等を用いたボンディングシートを貼り合わせた後にレーザーを用いて穴を加工しても良い。

【0043】また、保護層として異方性導電シートを用

いても良い。この場合には、絶縁層をパターンニングして形成し、更にパンプ電極を形成した後、絶縁層とパンプ電極を覆って異方性導電シートを貼り合わせることで、保護層を形成する。このようなチップ素子を回路基板に実装した場合には、異方性導電シートを全面で接着させることができるため、気密の漏れの無いシール性が得られる。

【0044】さらに、上記実施の形態において、パンプ電極は、先端頭部が平坦面である場合を例示したが、中央部が凹んだ形状等でもよい。また、パンプ電極として基部に比して頭部が幅広の形状を例示したが、基部から先端頭部まで同じ太さの形状等でもよい。

【0045】上記実施の形態で示した構造とすれば、チップ素子の実装主面は保護層によって覆われることになるので、チップ素子のパンプ電極にははんだや金、導電性樹脂等、多種類の異なるパンプ材料を用いることができ、しかも、クリームはんだや導電性樹脂、金による超音波ボンディング等、多様な接続方式を使用できる。その結果、同一回路基板上に各種のチップ素子を実装する際に、あるチップ素子のはんだにより実装を行い、他のチップ素子は導電性接着剤による実装を行う等、多様なチップ素子を同一の回路基板上に同時に多様な接合方法で実装することができる。しかも、接合時の雰囲気や温度、リフロー条件、超音波ボンディング条件等も幅広く選定することができる。すなわち、本発明によれば、同一の回路基板上に複数の異なるチップ素子を自由に MCM 実装することが容易になるという優れた効果を生む。

【0046】なお、本実施の形態のチップ素子を回路基板上に MCM 実装した後に全体を外装樹脂で覆うこともできるので、保護層を省略乃至簡易なものとし、最終的に外側を樹脂封止すること等、多様な変形が可能である。

【0047】以上本発明の実施の形態について説明してきたが、本発明はこれに限定されることなく請求項の記載の範囲内において各種の変形、変更が可能なことは当業者には自明であろう。

【0048】

【発明の効果】以上説明したように、本発明によれば、装着側基板上にフェースダウン実装されるチップ素子の実装主面に設けた絶縁層の縁部に密接して外部電極を設けるようにしたので、チップ素子を小型化でき、しかも高い信頼性を備えた高密度実装が可能なチップ素子を提供することができる。また、本発明を表面弾性波素子に適用することにより、信頼性に優れた小型な表面弾性波素子を提供することができる。

【0049】さらに、本発明の製造方法によれば、絶縁層形成工程と絶縁層に接して外部電極を作製する外部電極形成工程を設けるようにしたので、微小な外部電極を有するチップ素子を形成することができるという効果がある。

## 【図面の簡単な説明】

【図 1】本発明の実施の形態であってチップ素子を回路基板にフェースダウン実装した状態を示す断面図である。

【図 2】実施の形態におけるチップ素子の正断面図である。

【図 3】同平面図である。

【図 4】チップ素子に設けたバンプ電極周辺の構造及びフェースダウンボンディングの手順を示す拡大断面図である。

【図 5】チップ素子の製造手順を示す説明図である。

【図 6】チップ素子の従来例を示す断面図である。

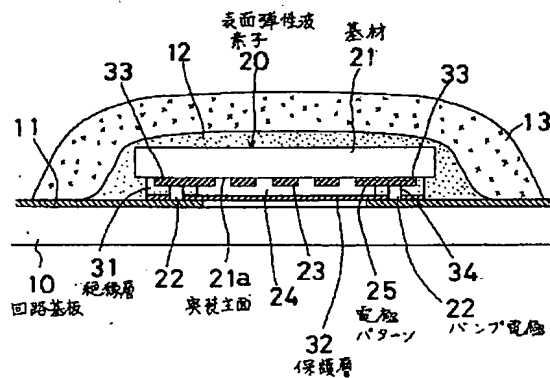
【図 7】同じく従来例を示す平面図である。

【図 8】チップ素子の他の従来例を示す平面図である。

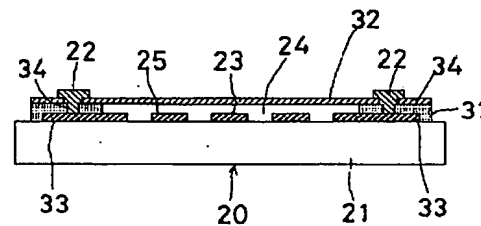
## 【符号の説明】

- 1, 20 表面弾性波素子  
2, 22 バンプ電極  
3, 23 楕形電極  
4, 24 活性領域  
10 回路基板  
11 導体パターン  
12 パッファ樹脂  
13 外装樹脂  
21 圧電基板  
21a 実装主面  
25 電極パターン  
31 絶縁層  
32 保護層  
33 パッド  
34 穴

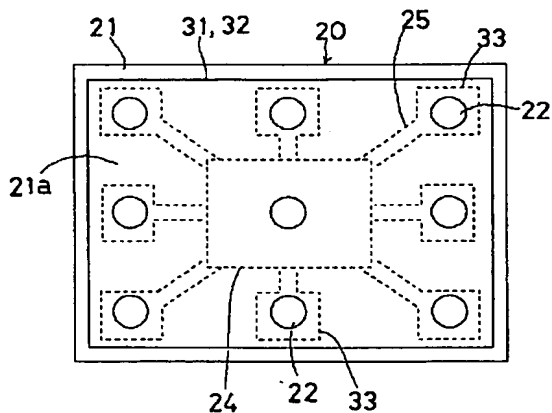
【図 1】



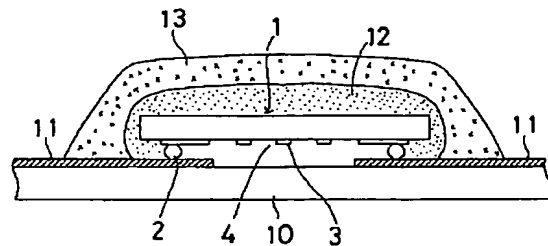
【図 2】



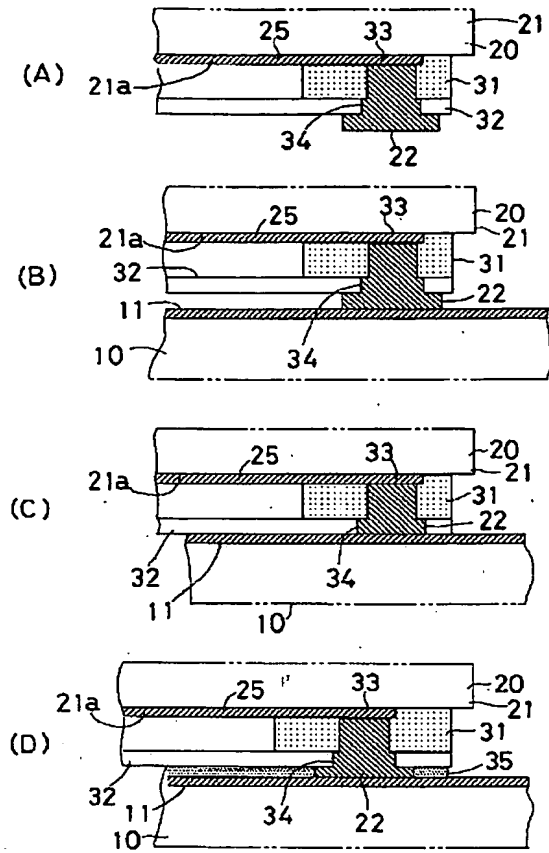
【図 3】



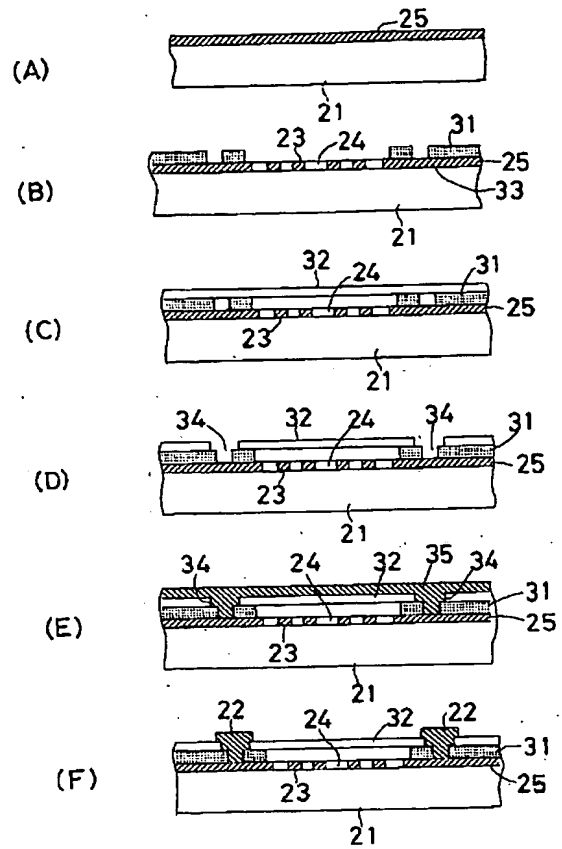
【図 6】



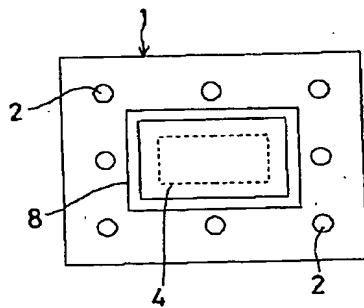
【図 4】



【図 5】



【図 7】



【図 8】

